IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Jerrell Hein		
Title:	RECONFIGURABLE TERMINAL		
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Examiner:	Richard B. Franklin	Group Art Unit:	2181
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RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF (37 C.F.R. § 41.37)

This paper is responsive to the Notification of Non-Compliant Appeal Brief mailed on December 14, 2007, having a period for response set to expire January 14, 2008. Applicant respectfully submits the attached SUMMARY OF CLAIMED SUBJECT MATTER as a replacement for the SUMMARY OF CLAIMED SUBJECT MATTER included in the Appeal Brief filed on November 28, 2007. While Applicant believes the original SUMMARY OF CLAIMED SUBJECT MATTER complies with the requirements of 37 CFR § 41.37(c)(1)(v) to provide a concise explanation of the independent claims on appeal, Applicant has revised the SUMMARY OF CLAIMED SUBJECT MATTER to further clarify the relationship between the description in the specification and drawings and claims 1, 10, 11, and 19. Applicant believes that the updated Appeal Brief complies with 37 C.F.R. § 41.37. Consideration of the updated Appeal Brief is respectfully requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 50-0631.

SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims involved in this appeal are claims 1, 10, 11, and 19. Independent claim 1 is directed to an apparatus including a terminal and control circuitry coupled to the terminal. Embodiments of a terminal are illustrated by terminal 27 in Figs. 1, 2, and 3, and are described at least in paragraphs 1019-1031. Other embodiments of the terminal are illustrated by P2 Port 82 in Fig. 4 and are described at least in paragraphs 1032-1034. Embodiments of control circuitry are illustrated by control circuit 30 and nonvolatile memory 60 of Figs. 3 and 4 and are described at least in paragraphs 1027-1037.

Independent claim 10 is directed to an apparatus including a terminal, control circuitry coupled to the terminal, and a second terminal. Embodiments of a terminal are illustrated by terminal 27 in Figs. 1, 2, and 3, and are described at least in paragraphs 1019-1031. Other embodiments of the terminal are illustrated by P2 Port 82 in Fig. 4 and are described at least in paragraphs 1032-1034. Embodiments of control circuitry are illustrated by control circuit 30 and nonvolatile memory 60 of Figs. 3 and 4 and are described at least in paragraphs 1027-1037. Embodiments of a second terminal are illustrated by P1 port 81 in Fig. 4 and are described at least in paragraphs 1032.

Independent claim 11 is directed to a method including utilizing a terminal in a first mode and subsequently permanently converting the terminal to a second mode. Descriptions of utilizing a terminal in a first mode are included at least in Figs. 5-7 and paragraphs 1027-1030, 1032, 1035-1037, 1046, and 1047. Descriptions of subsequently permanently converting the terminal to a second mode are included at least in paragraphs 1027, 1028, 1032, and 1033.

Independent claim 19 is directed to an apparatus including a terminal. Corresponding structures include OE terminal 27 of Figs. 1, 2, and 3 and P2 port 82 of Fig. 4, which are described at least in paragraphs 1019-1034. The apparatus also includes a means for permanently converting the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions as a control input to selectively enable an output according to a voltage value on the terminal, wherein the means for permanently converting is responsive to a serial

communication received over the terminal to convert the terminal to the second mode of operation. Exemplary read and write formats for serial communications are described in Fig. 5 and at least in paragraph 1035. A structure corresponding to the apparatus includes control circuit 30 and nonvolatile memory 60 of Fig. 3 and Fig. 4, which is described at least in paragraphs 1027-1037.

Referring to Fig. 1, realizations of the claimed subject matter include an integrated circuit 10 coupled to a crystal 11 or other resonating device. See paragraph 1019; Fig. 1. Both the integrated circuit 10 and the crystal 11 are packaged in a standard ceramic package 15 that is typically utilized for packaging a voltage controlled crystal oscillator (VCXO). See paragraph 1019; Fig. 1. The package 15 includes standard input/output signals including a voltage control input 17, a power and ground input, 19 and 21 respectively, clock out plus and minus 23 and an output enable pin and terminal 27. See paragraph 1019; Fig. 1.

In order to provide a more flexible clock device, according to an embodiment of the present invention, the OE pin 27 is multi-functional. See paragraph 1024. That is, in one embodiment, the OE terminal functions as a normal enable signal causing the output clock(s) to be either supplied or not according to the voltage level on the OE terminal. See paragraph 1024. In addition, according to an embodiment of the present invention, the OE terminal 27 is also used for programming and calibrating the device 10. See paragraph 1024. In order to program the integrated circuit device, the OE terminal 27 is used to communicate serial data to and from the integrated circuit 10. See paragraph 1024. Thus, in addition to normal enable/disable functionality, in one embodiment of the invention, the OE pin 27 serves as a serial port for access to storage locations internal to integrated circuit 10, thus providing programmability. See paragraph 1024. In an embodiment, the OE pin is bi-directional, implemented as an open drain with a weak pull-up. In some embodiments, the serial communication may be unidirectional into integrated circuit 10. See paragraph 1024.

Adapting the OE terminal to be multi-functional provides both programmability and calibration capability, and because a standard input terminal is utilized for the functions, no special packaging is required, resulting in low cost for the additional functionality. See paragraph 1026. Significantly, the functions can be performed after the device is packaged and

sealed. In addition, low frequency test equipment can be used to provide programming and calibration of the devices in a sealed package without any additional package pins. See paragraph 1026.

Referring to Fig. 3, a block diagram illustrates an embodiment of integrated circuit 10 utilized in a six pin VCXO package implementation. See paragraph 1027. In the illustrated embodiment, implementing the multi-functional OE terminal 27 is accomplished as follows. See paragraph 1027. The output enable signal supplied from an external source to OE terminal 27 is provided to control circuit 30, which may include a sampling circuit and a state machine. See paragraph 1027. The control circuit 30 determines whether the received signal is a valid output enable signal, serial data communication, or a calibration clock. See paragraph 1027. If the signal on OE terminal 27 is determined to be a valid output enable signal, then the signal value on OE pin 27 is utilized to generate an internal output enable control signal 31, which in turn enables (or disables) output drivers 33 that supply the differential clock outputs CLKOUT+ and CLKOUT-. See paragraph 1027.

Referring to Fig. 4, in another embodiment the option is provided for using one of two dedicated I/Os on the integrated circuit device. See paragraph 1032. The P1 port 81 is a dedicated I/O that functions as a bidirectional serial port for register data reads and writes, and as a calibration clock input, similar to the function of the OE pin used for programming and calibration described above but without any OE pin functionality. See paragraph 1032. The P2 port 82 is also a dedicated I/O with the same serial bus and calibration clock functionality as P1; however, once programming is completed, P2 can be converted from a dedicated serial port I/O to an input control for the output enable function. See paragraph 1032. Until the dedicated I/O functionality is disabled on P2, there is no output enable pin functionality provided by P2. See paragraph 1032. At the initiation of manufacture test, before the on-chip non-volatile memory (NVM) has been written, either P1 and P2 are able to receive serial bus and calibration clock signals as dedicated I/Os (both should not be used at the same time). See paragraph 1032. At the completion of the manufacture test programming of the various programmable registers, the user may write the programmable register values into non-volatile memory. P2 can then be programmed to function as an output enable control input causing its dedicated programmable I/O functionality to be permanently disabled. See paragraph 1032. That may be accomplished

by writing a keyword byte to a programmable register (activate output enable register) to turn on the output enable functionality of the P2 pin and terminate the dedicated serial I/O functionality of the P2 I/O. See paragraph 1032. That may be accomplished using logic gates enabling one function and disabling the other function according to the active output enable register value. See paragraph 1032. P1 always is available to function as a serial and calibration clock port. See paragraph 1032.

Writing the activate output enable register may cause the value to be written into the non-volatile memory (NVM). See paragraph 1033. Alternatively, a specific command may cause the value in the activate output enable register (and other volatile storage) to be written into the NVM. See paragraph 1033. Once the activate output enable register byte has been written into the non-volatile memory (NVM) with the appropriate keyword byte, the P2 I/O functions as the output enable input which controls the state of the clock output buffer. See paragraph 1033. If the NVM is one-time programmable, the change is permanent. See paragraph 1033. On power up or reset, the value in the NVM is loaded into the register to control the function of P2. See paragraph 1033. The active polarity of the P2 I/O when it has been programmed to function as an output enable pin may be controlled by programmable register bits. See paragraph 1033.

The serial port is typically used during manufacture test to establish the desired device configuration in the on-chip non-volatile memory (NVM) 60. See paragraph 1035. Serial port communications can begin following a power-on-reset of the device. An exemplary command format for the serial bus is shown in Fig. 5. See paragraph 1035. Each transmission consists of 3 eight bit bytes of data: the preamble byte 501, the instruction byte 503, and the address/data byte 505. See paragraph 1035. One extra clock cycle 507 exists for the Read command in order to allow time for placing the transmit output of the test equipment hooked up to the device in high impedance before the first read bit is sent by the device. See paragraph 1035. The serial port state machine, which may be part of deglitching circuit 83, returns to its initialized condition if any invalid input data is detected or if no activity occurs on the bus. See paragraph 1035. That feature guarantees that the state machine can always be brought to a known condition before signaling begins. See paragraph 1035.

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